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10/771,790	02/03/2004	David A. Williams	200300699-1	3345

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EXAMINER

CHOI, WILLIAM C

ART UNIT	PAPER NUMBER
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2873

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

Office Action Summary	Application No. 10/771,790	Applicant(s) WILLIAMS ET AL.	
	Examiner William C. Choi	Art Unit 2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>0204</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Information Disclosure Statement

Receipt of the Information Disclosure Statement (IDS) with copies of the references cited therein, was received on 2/3/2004. An initialized copy of the IDS is enclosed with this office action.

Claim Objections

Claim 37 is objected to because of the following informalities: in line 4, "having **and ON**" should be changed to "having **an ON**". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 31, 32 (and dependent claim 33) and 35 recite the limitation "the display device" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim. For purposes of examination, it was assumed that independent claim 30 was supposed to include a disclosure of a display device. (i.e. in line 1, "instructions for operating a display device"). Claim 33 inherits the rejection from its parent claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-14, 16-21 and 24-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Muraji et al (U.S. 5,134,491).

In regard to claim 1, Muraji et al discloses a display device (column 1, lines 7-10, Figure 1), comprising: an image formation apparatus (column 3, line 31, Figure 1, "3"), and a controller operably connected to the image formation apparatus (column 3, lines 61-63, Figure 1, "7"), configured to perform a power down process after a predetermined delay period in response to a receipt of a first power command, and to not perform the power down process in response to a receipt of a second power command prior to the end of the predetermined delay period (column 4, lines 29-55, Figure 2, " Δt_1 ").

Regarding claim 2, Muraji et al discloses wherein the image formation apparatus includes a light source (column 3, line 28, Figure 1, "1").

Regarding claim 3, Muraji et al discloses a lens adapted to focus light from the light source onto a projection surface in spaced relation to the display device (column 3, lines 31-32, Figure 1, "4").

Regarding claim 4, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

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Regarding claim 5, Muraji et al discloses wherein the image formation apparatus creates an image on the display surface (column 3, lines 27-32, Figure 1, "5") and wherein the controller is configured to control the image formation apparatus such that it is in an OFF state during the predetermined delay period (column 4, lines 37-41), wherein the image formation apparatus inherently would comprise a plurality of pixels, this being reasonably assumed from said image formation apparatus being disclosed as a liquid crystal display device forming an optical signal from a video signal (column 3, lines 32-35).

Regarding claim 6, Muraji et al discloses wherein the controller is configured to control the image formation apparatus such that the pixels are returned to an ON state in response to the receipt of a second power command prior to the end of the predetermined delay period (column 4, lines 42-50).

Regarding claim 8, Muraji et al discloses a power button that generates the first and second power commands (column 4, lines 29-47, Figure 1, "10").

Regarding claim 9, Muraji et al discloses wherein the power button is associated with a remote control (column 4, lines 33-37).

In regard to claim 10, Muraji et al discloses a display device (column 1, lines 7-10, Figure 1), comprising: an image formation apparatus (column 3, line 31, Figure 1, "3"), including a light source having an ON state and an OFF state (column 3, line 28, Figure 1, "1"); and a controller, operably connected to the image formation apparatus (column 3, lines 61-63, Figure 1, "7"), configured to (1) switch the light source to the ON state in response to a first power command (column 3, lines 59-67, Figure 1, "1"), (2) switch the image formation apparatus to the OFF state (column 4, lines 37-41) and to

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maintain the light source in the ON state in response to a second power command (column 4, lines 56-62), and (3) switch the light source to the OFF state in response to a failure of a third power command to be received within a predetermined delay period after second power command (column 4, lines 29-33), wherein the image formation apparatus inherently would comprise a plurality of pixels having an ON state and an OFF state, this being reasonably assumed from said image display device being disclosed as a liquid crystal display device forming an optical signal from a video signal (column 3, lines 32-35).

Regarding claim 11, Muraji et al discloses a lens adapted to focus light from the light source onto a projection surface in spaced relation to the display device (column 3, lines 31-32, Figure 1, "4").

Regarding claim 12, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

Regarding claim 13, Muraji et al discloses wherein the controller is configured to switch all of the pixels to the OFF state in response to the second power command (column 4, lines 37-41).

Regarding claim 14, Muraji et al discloses wherein the controller is configured to switch the pixels to the ON state and to maintain the light source in the ON state in response to a receipt of a third power command within the predetermined delay period after second power command (column 4, lines 42-50).

In regard to claim 16, Muraji et al discloses a display device (column 1, lines 7-10, Figure 1), comprising: means for supplying having an ON state and an OFF state (column 3, line 28, Figure 1, "1"); means for creating a plurality of pixels having an ON

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state and an OFF state with the light (column 3, line 31, Figure 1, "3"), means for switching at least a substantial majority of the pixels to the OFF state (column 3, lines 61-63, Figure 1, "7" and column 4, lines 37-41), while maintaining the means for supplying the light in the ON state, in response to a first power command (column 3, lines 59-67, Figure 1, "1"); and means for switching the means for supplying light to the OFF state in response to a failure of a second power command to be received within a predetermined delay period after first power command (column 3, lines 61-63, Figure 1, "7" and column 4, lines 29-33).

Regarding claim 17, Muraji et al discloses wherein the means for switching comprises means for switching all of the pixels to the OFF state, while maintaining the means for supplying light in the ON state, in response to a first power command (column 3, lines 61-63, Figure 1, "7", column 4, lines 37-41 & and 56-62).

Regarding claim 18, Muraji et al discloses a display device (column 1, lines 7-10, Figure 1), comprising: means for forming images (column 3, line 31, Figure 1, "3"); and means operably connected to the means for forming images (column 3, lines 61-63, Figure 1, "7"), for performing a power down process after a predetermined delay period in response to a receipt of a first power command, and not performing the power down process in response to a receipt of a second power command prior to the end of the predetermined delay period (column 4, lines 29-55, Figure 2, " Δt_1 ").

In regard to claim 19, Muraji et al discloses a method of operating a display device (column 1, lines 7-10, Figure 1), comprising the steps of: switching a light source to an ON state in response to a first power command (column 3, lines 59-67, Figure 1, "1"); directing light from the light source onto a display surface (column 3, lines 27-32,

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Figure 1, "5"); preventing the light from the light source from being directed onto the display surface, while maintaining the light source in the ON state, in response to a second power command (column 4, lines 29-40); and switching the light source to an OFF state in response to a failure of a third power command to be received within a predetermined delay period after second power command (column 4, lines 29-33, Figure 2, "T₅").

Regarding claim 20, Muraji et al discloses maintaining the light source in the ON state in response to the receipt of the third power command within the predetermined delay period after second power command (column 4, lines 42-50, Figure 2, "T₃").

Regarding claim 21, Muraji et al discloses directing light from the light source onto the display surface in response to the receipt of the third power command within the predetermined delay period after second power command (column 4, lines 42-50, Figure 2, "T₃").

Regarding claim 22, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

Regarding claim 24, Muraji et al discloses wherein the step of projecting light comprises projecting an image onto a screen (column 3, lines 27-32, Figure 1, "5").

In regard to claim 25, Muraji et al discloses a method of operating a display device (column 1, lines 7-10, Figure 1), comprising the steps of: performing a power down process after a predetermined delay period in response to a receipt of a first power command (column 4, lines 29-33, Figure 2, "T₅"); and not performing the power down process in response to a receipt of a second power command prior to the end of the predetermined delay period (column 4, lines 42-50, Figure 2, "T₃").

Regarding claim 26, Muraji et al discloses switching the image formation apparatus to an OFF state in response to the first power command (column 4, lines 37-41), wherein the image formation apparatus inherently would comprise a plurality of pixels, this being reasonably assumed from said image formation apparatus being disclosed as a liquid crystal display device forming an optical signal from a video signal (column 3, lines 32-35).

Regarding claim 27, Muraji et al discloses switching the image formation apparatus to an ON state in response to the receipt of the second power command prior to the end of the predetermined delay period (column 4, lines 42-50), wherein the image formation apparatus inherently would comprise a plurality of pixels, this being reasonably assumed from said image formation apparatus being disclosed as a liquid crystal display device forming an optical signal from a video signal (column 3, lines 32-35).

Regarding claim 28, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

Regarding claim 29, Muraji et al discloses wherein the step of performing a power down process includes the step of turning a light source to an OFF state (column 4, lines 29-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7, 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muraji et al in view of Noji et al (U.S. 6,543,900 B2)

Regarding claims 7, 15 and 23, Muraji et al discloses as set forth above respectively in claims 1, 10 and 19, but does not specifically disclose wherein the image formation apparatus includes a plurality of mirrors and wherein the step of directing light from the light source onto a display surface comprises reflecting light from the light source onto a display surface by turning a plurality of mirrors toward the light source; and the step of preventing the light from the light source from being directed onto the display surface comprises turning the plurality of mirrors away from the light source.

However, Muraji et al teaches wherein any device that displays images due to variation of its optical characteristics by an electrical signal may be used as the image formation apparatus (column 4, lines 63-68) and within the same field of endeavor, Noji et al teaches that it is well known in the art of projectors for image formation apparatuses to comprise liquid crystal devices or micromirror rocking pixel devices which inherently perform the reflection steps as claimed (column 1, lines 11-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

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invention was made for the image formation apparatus to comprise a plurality of mirrors as claimed since Muraji et al teaches wherein any device that displays images due to variation of its optical characteristics by an electrical signal may be used as the image formation apparatus and within the same field of endeavor, Noji et al teaches that it is well known in the art of projectors for image formation apparatuses to comprise liquid crystal devices or micromirror rocking pixel devices.

Claims 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muraji et al in view of Tanenbaum ("Structured Computer Organization Publication").

In regard to claim 30, Muraji et al discloses instructions for operating a display device (column 1, lines 7-10, Figure 1) comprising steps for: performing a power down process after a predetermined delay period in response to a receipt of a first power command (column 4, lines 29-33, Figure 2, "T₅"); and not performing the power down process in response to a receipt of a second power command prior to the end of the predetermined delay period (column 4, lines 42-50, Figure 2, "T₃"), but does not specifically disclose computer memory encoded with said instructions.

Within the field of computer memory, Tanenbaum teaches wherein hardware and software are logically equivalent and any instruction executed by hardware can be simulated in software (page 11, paragraph 3). Therefore, it would have been obvious for the instructions of Muraji et al to be encoded in computer memory since Tanenbaum teaches wherein hardware and software are logically equivalent and any instruction executed by hardware can be simulated in software.

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Regarding claim 31, Muraji et al discloses wherein the display device includes a light source (column 3, line 27, Figure 1, "1") and the step of performing a power down process includes placing the light source in an OFF state (column 4, lines 29-33).

Regarding claim 32, Muraji et al discloses wherein the step of performing a power down process includes maintaining the light source in an ON state during the predetermined delay period (column 4, lines 56-62).

Regarding claim 33, Muraji et al discloses wherein the step of not performing the power down process includes maintaining the light source in the ON state after the end of the predetermined delay period (column 4, lines 42-50).

Regarding claim 34, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

Regarding claim 35, Muraji et al discloses wherein an image is created on the display surface (column 3, lines 27-32, Figure 1, "5") and wherein the image formation apparatus is in an OFF state during the predetermined delay period (column 4, lines 37-41), wherein the image formation apparatus inherently would comprise a plurality of pixels, this being reasonably assumed from it being disclosed as a liquid crystal display device forming an optical signal from a video signal (column 3, lines 32-35).

Regarding claim 36, Muraji et al discloses wherein the first and second power commands comprise signals from a power button (column 4, lines 29-47, Figure 1, "10").

In regard to claim 37, Muraji et al in view of Tanenbaum discloses instructions for operating an image formation apparatus display device (column 1, lines 7-10, Figure 1), the image formation apparatus being adapted to produce a plurality of pixels having an

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ON and an OFF state (column 3, lines 32-35, Figure 1, "3") and including a light source having an ON state and an OFF state (column 3, line 28, Figure 1, "1"), the instructions comprising steps for: switching the light source to an ON state in response to a first power command (column 3, lines 59-67, Figure 1, "1"); switching at least a substantial majority of the pixels to the OFF state (column 4, lines 37-41) and for maintaining the light source in the ON state in response to a second power command (column 4, lines 56-62); and switching the light source to the OFF state in response to a failure of a third power command to be received within a predetermined delay period after second power command (column 4, lines 29-33), but does not specifically disclose computer memory encoded with said instructions.

Within the field of computer memory, Tanenbaum teaches wherein hardware and software are logically equivalent and any instruction executed by hardware can be simulated in software (page 11, paragraph 3). Therefore, it would have been obvious for the instructions of Muraji et al to be encoded in computer memory since Tanenbaum teaches wherein hardware and software are logically equivalent and any instruction executed by hardware can be simulated in software.

Regarding claim 38, Muraji et al discloses wherein the predetermined delay period is at least two seconds (column 4, lines 53-55, Figure 2, " Δt_1 ").

Regarding claim 39, Muraji et al discloses wherein the step of switching at least a substantial majority of the pixels to the OFF state switch all of the pixels to the OFF state (column 4, lines 37-41).

Regarding claim 40, Muraji et al discloses switching the pixels to an ON state and maintaining the light source in an ON state in response to a receipt of a third power

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command within the predetermined delay period after second power command (column 4, lines 42-50).

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Choi whose telephone number is (571) 272-2324. The examiner can normally be reached on Monday-Friday from about 9:00 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Y. Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W.C.

William Choi
Patent Examiner
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April 12, 2005


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